

CLAIM LISTING

This listing of claims, if entered, replaces all prior versions of the claims in the application.

1. (Currently Amended) A method, comprising:
detecting a timing violation, caused by crosstalk, in a timing path included in an integrated circuit design;
removing one of one or more wires included in the timing path, wherein the one of the one or more wires couples two nodes included in the integrated circuit design; and
routing a new wire between the two nodes, wherein the new wire is longer than the removed one of the one or more wires, and wherein the new wire experiences fewer crosstalk effects than the removed one of the one or more wires.
2. (Original) The method of claim 1, wherein
the new wire is routed through a higher routing layer than the removed one of the one or more wires.
3. (Original) The method of claim 1, further comprising:
calculating timing information for the one or more wires included in the timing path; and
selecting the one of the one or more wires for removal dependent on the timing information.
4. (Original) The method of claim 3, wherein
the timing information includes delay information.
5. (Original) The method of claim 4, further comprising:
selecting the one of the one or more wires for removal in response to the delay information indicating that the one of the one or more wires has a greater delay than other ones of the one or more wires included in the timing path.
6. (Original) The method of claim 5, further comprising:

selecting the one of the one or more wires to remove in response to the delay information indicating that a delay of the one of the one or more wires exceeds a threshold delay.

7. (Original) The method of claim 3, wherein the timing information includes slew information.

8. (Original) The method of claim 3, wherein the timing information includes both slew information and delay information for each of the one or more wires included in the timing path.

9. (Original) The method of claim 8, further comprising:
sorting the one or more wires included in the timing path based on the slew information and the delay information;
dependent on an outcome of said sorting, selecting the one of the one or more wires for removal.

10. (Original) The method of claim 3, further comprising:
sorting the one or more wires dependent on the timing information; and
selecting the one of the one or more wires for removal in response to said sorting.

11. (Original) The method of claim 1, wherein said removing is dependent on a location of the one of the one or more wires relative to one or more other wires included in the integrated circuit design.

12. (Currently Amended) The method of claim 11, further comprising:
selecting the one of the one or more wires for removal in response to determining that the one of the one or more wires has fewer neighboring wires than a second one of the one or more wires ~~a different one of the one or more wires has so many neighboring wires that if the different one of the one or more wires is replaced with a new wire, the new wire is likely to cause additional timing violations due to crosstalk with one of the neighboring wires.~~

13. (Original) The method of claim 1, wherein said detecting is performed by a sign-off tool.
14. (Original) The method of claim 1, further comprising:
removing more than one of the one or more wires included in the timing path, wherein
each of the more than one of the one or more wires couples a respective pair of a plurality of pairs of nodes; and
routing a new wire between each pair included in the plurality of pairs of nodes.
15. (Currently Amended) The method of claim 1, wherein
said routing comprises routing the new wire so that a space exists between the new wire
and any other wires, wherein
a size of the space is selected to reduce ~~a likelihood that the new wire will experience~~
crosstalk effects between the new wire and one or more ~~with any~~ other wires.
16. (Original) The method of claim 1, wherein
the new wire has less delay and less slew than the one of the one or more wires removed
by said removing.
17. (Original) The method of claim 1, wherein
a driver for driving signals on the new wire has substantially a same size as a driver for
driving signals on the one of the one or more wires removed by said removing.
18. (Original) The method of claim 1, wherein
said routing does not introduce any new timing violations into the integrated circuit
design.
19. (Original) The method of claim 1, further comprising:
performing said detecting, said removing, and said routing for a plurality of additional
timing paths, wherein

no new buffers are added, no existing drivers are resized, and no existing buffers are resized or moved in response to detection of the timing violations in the timing path and the plurality of additional timing paths; and subsequent to said performing, no timing violations are detected in a circuit design that includes the timing path and the plurality of additional timing paths.

20. (Original) The method of claim 19, wherein a single wire is selected as the one of the one or more wires to be removed for more than one timing path of the plurality of additional timing paths.

21. (Currently Amended) A system, comprising:
a processor; and
a memory coupled to the processor and storing program instructions executable by the processor to:
detect a timing violation[[s]], caused by crosstalk, in a timing path included in an integrated circuit design;
remove one of one or more wires included in the timing path, wherein the one of the one or more wires couples two nodes; and
route a new wire between the two nodes, wherein the new wire is longer than the removed one of the one or more wires, and wherein the new wire experiences fewer crosstalk effects than the removed one of the one or more wires.

22. (Original) The system of claim 21, wherein the program instructions are executable to:
route the new wire through a higher routing layer than the removed one of the one or more wires.

23. (Original) The system of claim 21, wherein the program instructions are executable to:
calculate timing information for the one or more wires; and

dependent on the timing information, select the one of the one or more wires for removal.

24. (Original) The system of claim 23, wherein the timing information includes delay information.

25. (Original) The system of claim 24, wherein the program instructions are executable to:
select the one of the one or more wires to remove in response to the delay information indicating that a delay of the one of the one or more wires exceeds a threshold delay.

26. (Original) The system of claim 23, wherein the timing information includes slew information.

27. (Original) The system of claim 23, wherein the program instructions are executable to:
sort the plurality of wires dependent on the timing information.

28. (Original) The system of claim 21, wherein the program instructions are executable to:
remove the one of the one or more wires dependent on a location of the one of the one or more wires relative to one or more other wires.

29. (Original) The system of claim 21, wherein the program instructions are executable to:
remove more than one of the one or more wires included in the timing path, wherein each of the more than one of the one or more wires couples a respective pair of a plurality of pairs of nodes; and
route a new wire between each pair included in the plurality of pairs of nodes.

30. (Currently Amended) The system of claim 21, wherein the program instructions are executable to:

route the new wire so that a space exists between the new wire and any other wires,
wherein
a size of the space is selected to reduce ~~a likelihood that the new wire will~~
~~experience crosstalk effects~~ between the new wire and one or more with
~~any other wires.~~

31. (Original) The system of claim 21, wherein
the new wire has less delay and less slew than the removed one of the one or more wires.

32. (Original) The system of claim 21, wherein
a driver for driving signals on the new wire has substantially a same size as a driver for
driving signals on the removed one of the one or more wires.

33. (Original) The system of claim 21, wherein the program instructions are
executable to:
route the new wire without introducing any new timing violations into the integrated
circuit design.

34. (Currently Amended) A computer readable medium comprising program
instructions executable to:
detect a timing violation[[s]], caused by crosstalk, in a timing path included in the
integrated circuit design;
remove one of one or more wires included in the timing path, wherein the one of the one
or more wires couples two nodes; and
route a new wire between the two nodes, wherein the new wire is longer than the
removed one of the one or more wires, and wherein the new wire experiences
fewer crosstalk effects than the removed one of the one or more wires.

35. (Original) The computer readable medium of claim 34, wherein the program
instructions are executable to:
route the new wire through a higher routing layer than the removed one of the one or
more wires.

36. (Original) The computer readable medium of claim 34, wherein the program instructions are executable to:

calculate timing information for the one or more wires included in the timing path; and dependent on the timing information, select the one of the one or more wires for removal.

37. (Original) The computer readable medium of claim 36, wherein the timing information includes delay information.

38. (Original) The computer readable medium of claim 37, wherein the program instructions are executable to:

select the one of the one or more wires to remove in response to the delay information indicating that a delay of the one of the one or more wires exceeds a threshold delay.

39. (Currently Amended) The computer readable medium of claim 37, wherein the program instructions are executable to:

select the one of the one or more wires to remove in response to the delay information indicating that ~~a delay of the one of the one or more wires exceeds a threshold~~ delay has a greater delay than other ones of the one or more wires included in the timing path.

40. (Original) The computer readable medium of claim 36, wherein the timing information includes slew information.

41. (Original) The computer readable medium of claim 36, wherein the program instructions are executable to:

sort the one or more wires dependent on the timing information.

42. (Original) The computer readable medium of claim 34, wherein the program instructions are executable to:

select the one of the one or more wires for removal dependent on a location of the one of the one or more wires relative to one or more other wires.

43. (Currently Amended) The computer readable medium of claim 42, wherein the program instructions are executable to:

select the one of the one or more wires for removal in response to determining that the one of the one or more wires has fewer neighboring wires than a second one of the one or more wires ~~a different one of the one or more wires has so many neighboring wires that if the different one of the one or more wires is replaced with a new wire, the new wire is likely to cause additional timing violations due to crosstalk with one of the neighboring wires.~~

44. (Original) The computer readable medium of claim 34, wherein the program instructions are executable to:

remove more than one of the one or more wires included in the timing path, wherein each of the more than one of the one or more wires couples a respective pair of a plurality of pairs of nodes; and
route a new wire between each pair included in the plurality of pairs of nodes.

45. (Currently Amended) The computer readable medium of claim 34, wherein the program instructions are executable to:

route the new wire so that a space exists between the new wire and any other wires,
wherein
a size of the space is selected to reduce ~~a likelihood that the new wire will experience crosstalk effects~~ between the new wire and one or more ~~with any other wires.~~

46. (Original) The computer readable medium of claim 34, wherein
the new wire has less delay and less slew than the removed one of the one or more wires.

47. (Original) The computer readable medium of claim 34, wherein
a driver for driving signals on the new wire has substantially a same size as a driver for driving signals on the removed one of the one or more wires.

48. (Original) The computer readable medium of claim 34, wherein

routing the new wire does not introduce any new timing violations into the integrated circuit design.

49. (Currently Amended) A computer readable medium, comprising program instructions executable to:

select one of a one or more wires included in a timing path included in an integrated circuit design for removal in response to a timing violation, caused by crosstalk, being detected in the timing path, wherein the one of the one or more wires couples two nodes in the integrated circuit design;

remove the one of the one or more wires selected by said selecting;

route a new wire between the two nodes, wherein the new wire is longer than the one of the one or more wires removed by said removing, and wherein the new wire experiences fewer crosstalk effects than the removed one of the one or more wires.

50. (Original) The computer readable medium of claim 49, wherein the program instructions are executable to:

select the one of the one or more wires dependent on timing information associated with each of the one or more wires.

51. (Currently Amended) A integrated circuit designed by a process, the process comprising:

detecting a timing violation, caused by crosstalk, in a timing path included in an integrated circuit design;

removing one of one or more wires included in the timing path, wherein the one of the one or more wires couples two nodes included in the integrated circuit design; and

routing a new wire between the two nodes, wherein the new wire is longer than the removed one of the one or more wires, and wherein the new wire experiences fewer crosstalk effects than the removed one of the one or more wires;

wherein the integrated circuit includes an empty space through which a shorter wire coupling the two nodes could have been placed during fabrication of the integrated circuit.

52. (Original) The integrated circuit of claim 51, wherein said routing the new wire comprises routing the new wire through a higher routing layer than the removed one of the one or more wires.

53. (Original) The integrated circuit of claim 51, wherein the process further comprises:
calculating timing information for the one or more wires included in the timing path; and
selecting the one of the one or more wires for removal dependent on the timing information.